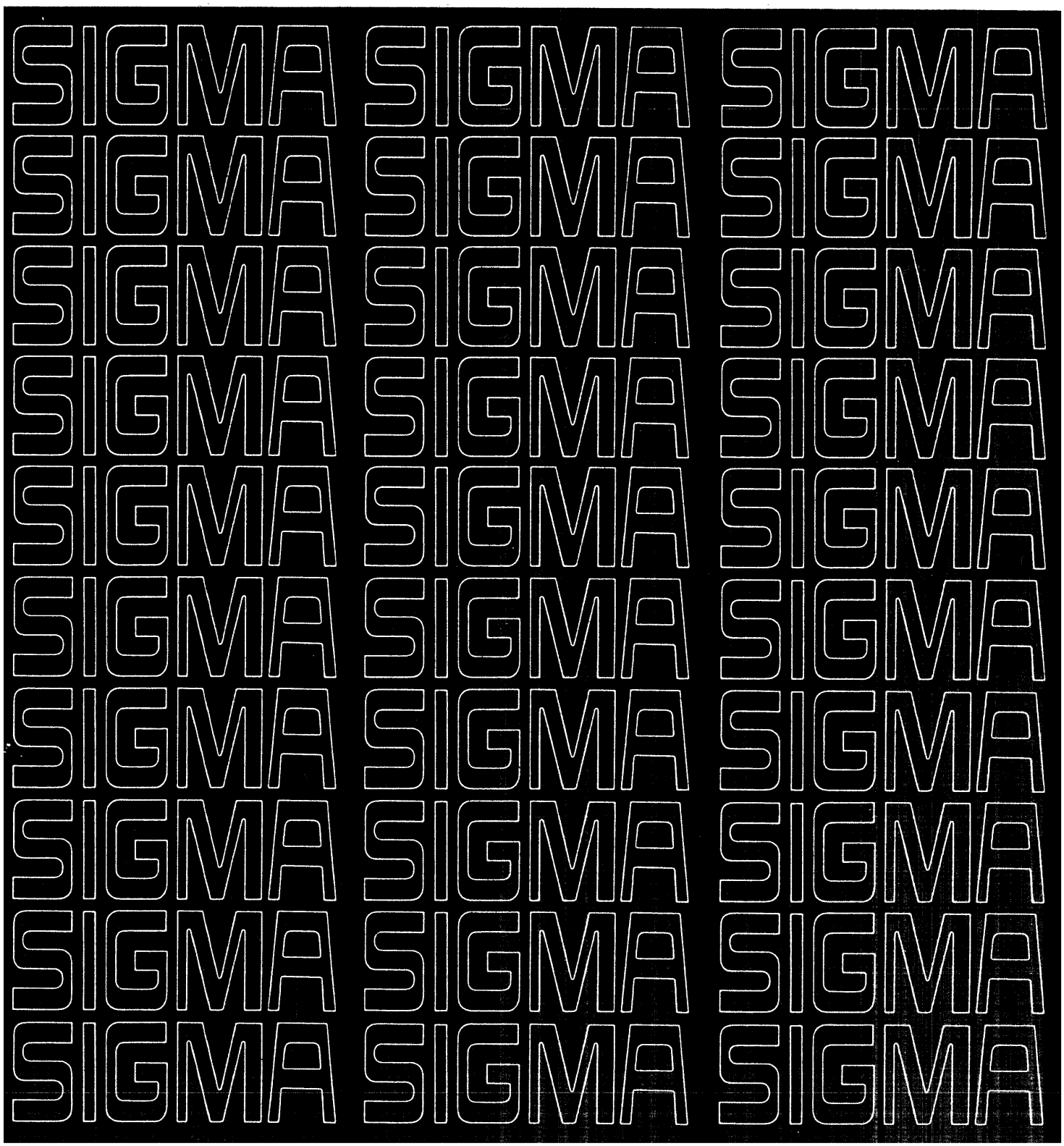
SDS

Scientific Data Systems
A XEROX COMPANY

SDS SIGMA 100 CARD/MINUTE CARD PUNCH
MODEL 7165

Reference Manual



CARD PUNCH ORDER CODES

Code (Hexadecimal)	Function
01	Punch Binary (stack card normally)
05	Punch EBCDIC (stack card normally)
09	Punch Binary (offset stack on error)
0D	Punch EBCDIC (offset stack on error)
11	Punch Binary (offset stack)
15	Punch EBCDIC (offset stack)
19	Punch Binary (offset stack)
1D	Punch EBCDIC (offset stack)
41†	Punch Binary (stack card normally)
45†	Punch EBCDIC (stack card normally)
49†	Punch Binary (offset stack on error)
4D†	Punch EBCDIC (offset stack on error)
51†	Punch Binary (offset stack)
55†	Punch EBCDIC (offset stack)
59†	Punch Binary (offset stack)
5D†	Punch EBCDIC (offset stack)

†Interrupt at Data Transmission Complete (i.e., device-initiated interrupt occurs at zero byte count).

PRICE: $1.00

100 CARD/MINUTE CARD PUNCH

MODEL 7165

REFERENCE MANUAL

for

SDS SIGMA COMPUTERS

PRELIMINARY EDITION

90 15 67A

July 1969

SDS

SCIENTIFIC DATA SYSTEMS A XEROX COMPANY/701 South Aviation Boulevard/El Segundo, California 90245

©1969, Scientific Data Systems, Inc.

Printed in U.S.A.

RELATED PUBLICATIONS

Title	Publication No.
SDS Sigma 7 Computer Reference Manual	90 09 50
SDS Sigma 5 Computer Reference Manual	90 09 59
SDS Sigma 2 Computer Reference Manual	90 09 64
SDS 5/7 Symbol and Meta-Symbol Reference Manual	90 09 52
SDS Sigma 2 Symbol Reference Manual	90 10 51

ALL SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

CONTENTS

1. GENERAL DESCRIPTION 1

Introduction 1

2. FUNCTIONAL DESCRIPTION 2

Physical Description 2
Data Presentation 2
EBCDIC Format 2
Binary Format 2
Card Punch States 3
Operational States 3
Ready Condition 3
Busy Condition 3
Manual Mode 3
Automatic Mode 3
Transition Between States 3
Data Transfer 3

3. PROGRAM INTERFACE 5

Punch Orders 5
Punch Card EBCDIC 5
Punch Card Binary 5
Key Events 5
Start Input/Output 5
Unusual End Conditions 5
Channel End Condition 6
Fault Conditions 6
Error Conditions 6
Card Punch Status Response 6
I/O Instruction Status Bits 6
Device Status Byte 6
Operational Status Byte 6
Programming Considerations 6

4. OPERATIONS 12

Operator Controls 12
Power 12
Start 12
Stop 13
Manual Feed 13
Reset 13
Hopper/Stacker 13
Punch Error 14
Chips/Jam 14
Input Hopper 14
Output Stacker 14
Cover Interlock 14
Operating Instructions 14
Operating Preparation 14
Turn-On Procedure 14
Continuous Operation 14
Momentary Halt 14
Automatic Recoverable Halt 14
Clearing Card Jams 15
Pick Jam 15
Throat Jam 15
Registration Jam 15
Eject Jam 16
Punch Head Jam 16

APPENDIXES

A. SDS STANDARD SYMBOLS, CODES, AND CORRESPONDENCES 17

B. PROGRAMMING EXAMPLES 23

Sigma 5/7 Programming Example 23
Sigma 2 Programming Example 24

ILLUSTRATIONS

Model 7165 Card Punch iv

1. Card Rate (cards per minute) 1
2. EBCDIC Card Punch Operation 2
3. Binary Card Punch Operation 2
4. Card Punch Timing 9
5. Controlling System and Card Punch Actions 10
6. Model 7165 Card Punch 12
7. Control Panel 13
8. Card Punch Mechanism with Access Cover Open 15
9. Card Punch Mechanism, Left View 16

TABLES

1. Characteristics 1
2. Card Punch State Transitions 4
3. Card Punch I/O Instruction Execution Response 6
4. Device Status Response for SIO, TIO, and HIO 7
5. Device Status Response for TDV and AIO 8
6. Operational Status Byte 8

Model 7165 Card Punch

1. GENERAL DESCRIPTION

INTRODUCTION

SDS Model 7165 Card Punch permits Sigma computer users to punch a standard 80-column card serially, column by column, at a rate of 100 cards per minute. When punching fewer than 80 columns, the rate increases up to a maximum of 300 cards per minute. Data is punched in either binary or EBCDIC format; an automatic check detects erroneously punched cards. An input hopper provides for card loading, and an output stacker for unloading. A card offset feature allows a selected card to be offset (raised) from the stack upon command. This feature may be used for card deck separation, for example.

When the card punch is operating, a card is picked from the input hopper and transported to the registration station where it is stopped and registered for column one data. After column one, the card is incrementally stepped, has as many columns punched as required, and then is transported to the output stacker. Photo-electric diodes monitor card progress through the transport and provide signals for transport control and card-handling malfunctions.

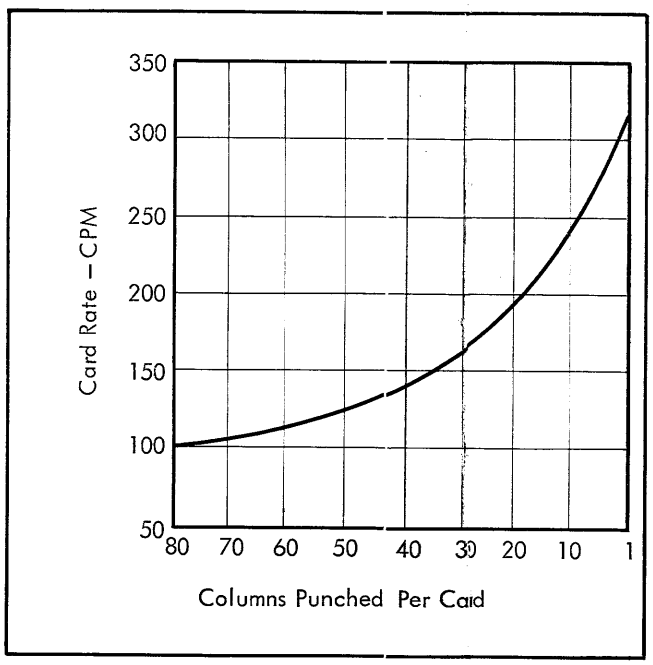


Figure 1. Card Rate (cards per minute)

Table 1. Characteristics

Operating Characteristics	
Punch Speed (See Figure 1)	100 cards per minute (all 80 columns)
	300 cards per minute (single column)
Hopper capacity	1000 cards
Stacker capacity	1000 cards
Card type	EIA standard RS-292, media I.
Physical Characteristics	
Height	40 in.
Width	37.5 in.
Depth	33 in.
Weight (approximate)	480 lb
Cable length (Controller to punch)	40 ft (standard) 200 ft (optional)
Environmental Characteristics	
Power requirements	120 vac ± 10%, 50 or 60 Hz ± 1%, single-phase
Initial surge	36 amp for 150 ms
Steady state	9.5 amp, idle; 16 amp, punching
Temperature	
Operating	50° F to 95° F
Shipping or storage	-40° F to 150° F
Humidity	
Operating	20% to 75%
Shipping or storage	20% to 95% (provided no condensation occurs)
Shock	5Gs for 11 ± 1 ms
Vibration	1G from 15 to 500 Hz

2. FUNCTIONAL DESCRIPTION

PHYSICAL DESCRIPTION

This card punch system consists of a card punch device with an electronics chassis assembly and a punch controller assembly (mounted in a standard SDS I/O rack). The controller interfaces the electronics chassis to the Sigma IOP or I/O channel.

The card punch is a free-standing unit, mounted on casters. The card-handling mechanism is supported on a rigid frame by vibration mounts. The front and rear doors and cover are hinged for easy access.

DATA PRESENTATION

An 80-column card may be used to record data in either of two formats, EBCDIC or binary.

EBCDIC FORMAT

In the EBCDIC format, a card image consists of from 1 to 80 bytes of data. Each byte of this image is an 8-bit code in the range 0 - 255_{10} (00_{16} - FF_{16}), each of which corresponds to a punch configuration for a single column (see Appendix A). This card image, when transmitted to the card punch, is recorded on the card column by column with the punch configuration in column 1 corresponding to the first transmitted byte of the card image and the punch configuration in the last column corresponding to the last byte of the card image.

Figure 2 illustrates how the first two bytes of an EBCDIC card image are presented to the card punch by the controlling system. Note that EBCDIC code 40_{16} produces a blank (no punch) card column.

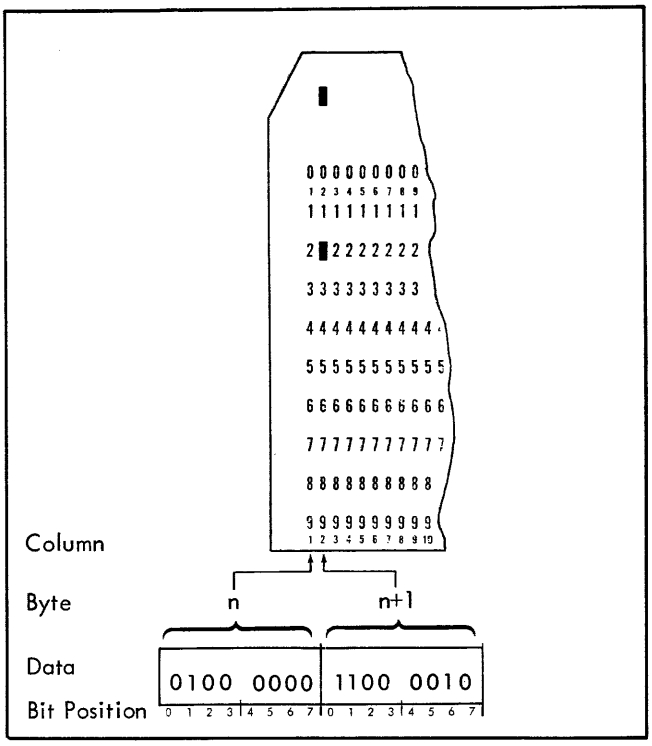


Figure 2. EBCDIC Card Punch Operation

BINARY FORMAT

In the binary format, a card image consists of from 1 to 120 bytes of data. The binary card image, when received by the card punch, is reassembled as 12-bit codes and each 12-bit code is punched in the corresponding card column.

Figure 3 illustrates how the first three bytes of a binary card image are punched. Note that the first byte of the binary card image is punched in column 1, rows 12-5, with a 1 in the byte corresponding to a punch in the appropriate row. The second byte of the card image is separated so that bits 0-3 of the byte correspond to punches in rows 6-9 of column 1, and bits 4-7 of the byte correspond to rows 12-1 of column 2. The third byte of the card image is punched in rows 2-9 of column 2.

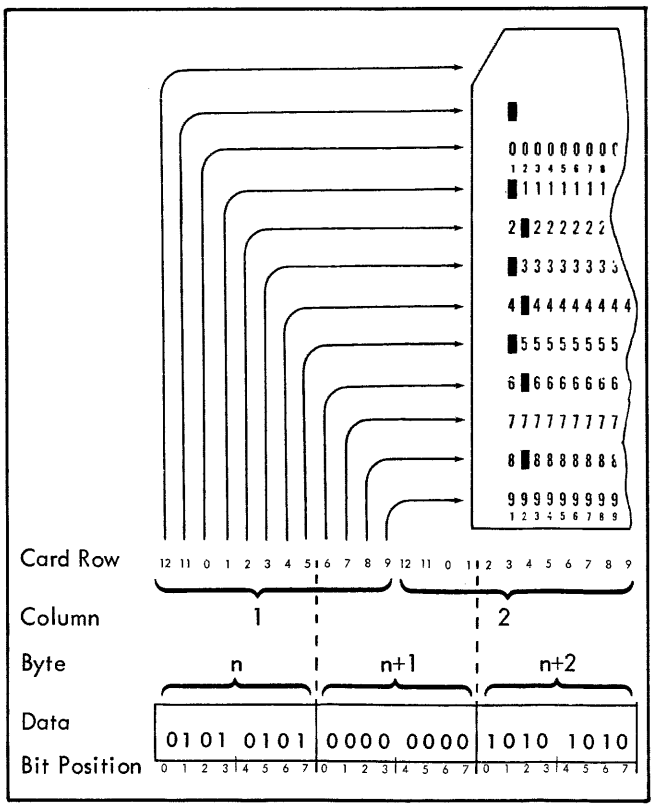


Figure 3. Binary Card Punch Operation

CARD PUNCH STATES

The initial state of the card punch depends on its power status. Complete absence of power removes the card punch from the controlling system. If power is applied to the controller, address recognition takes place when an I/O instruction is issued. If no power is applied to the punch when an I/O instruction is issued, status information is returned to the computer indicating the device is "not operational".

OPERATIONAL STATES

The card punch is in one of the four operational states explained below and summarized in Table 2 if the following conditions are satisfied.

1. Power is present.
2. No transport mechanism fault exists.
3. Interlock is closed.
4. No manual card feed is in process.

The condition and mode status of the card punch at any given time is returned to the central processor in response to such I/O instructions as SIO, HIO, and TIO. Other I/O instructions, such as AIO and TDV, obtain more specific indications of punch status.

READY CONDITION

In the "ready" condition, the punch can accept an SIO instruction, provided that no interrupt is pending. To be in the "ready" condition, the punch must be "operational" and the execution of an order to punch a card must not be pending.

BUSY CONDITION

In the "busy" condition, the punch has accepted an SIO instruction. It will not accept a new order until the current order (or orders) is completed and no interrupt is pending.

MANUAL MODE

The punch is in the "manual" mode when any condition requiring operator intervention arises before the punch can function normally (e.g., stacker full, hopper empty, or chip box full). The "manual" mode is forced by the operator pressing the STOP switch on the card punch control panel. The punch can accept an SIO instruction in this mode but does not act on it until the "automatic" mode is entered.

AUTOMATIC MODE

When all conditions for successful card punch operation are present, the punch enters the "automatic" mode when the START switch is pressed.

TRANSITION BETWEEN STATES

The card punch state transitions and the conditions causing the punch to change from one operational state to another are summarized in Table 2.

DATA TRANSFER

A card punch operation is initiated from the controlling system by an SIO instruction if the following conditions are satisfied.

1. I/O address recognition exists.
2. Punch is in "ready" condition.
3. No interrupt is pending.

If the card punch is in the "automatic" mode, it requests an order from the controlling system to punch one card. After receiving a valid punch order, the card punch begins to accept the card image, column by column, from the controlling system. Data for column 1 is received and punched, then data for column 2, and so on, for the entire card image until the punch receives a "count done" or "halt" signal or a fault condition is encountered. The byte count in the I/O command doubleword controls the number of columns to be punched. Normal or offset stacking is specified in the punch order. (See Chapter 3 for detailed information.)

Table 2. Card Punch State Transitions

Present State \ Next State	Ready Manual	Busy Manual	Ready Automatic	Busy Automatic
Ready Manual	———	SIO accepted, manual card feed in progress	START switch operated with no operator intervention† required	Not possible
Busy Manual	• I/O reset • HIO received • Device RESET switch operated • Invalid order • Manual feed complete	———	Not possible	START switch operated with no operator intervention† required
Ready Automatic	STOP or device RESET switch operated	Not possible	———	SIO accepted
Busy Automatic	• STOP switch operated and no order pending • Device RESET switch operated • Operation completed and no order pending but operator intervention† required	• STOP switch operated with order pending • Operation completed with order pending but operator intervention† required	• I/O reset • HIO received • Invalid order • Operation completed and no operator intervention† required	———

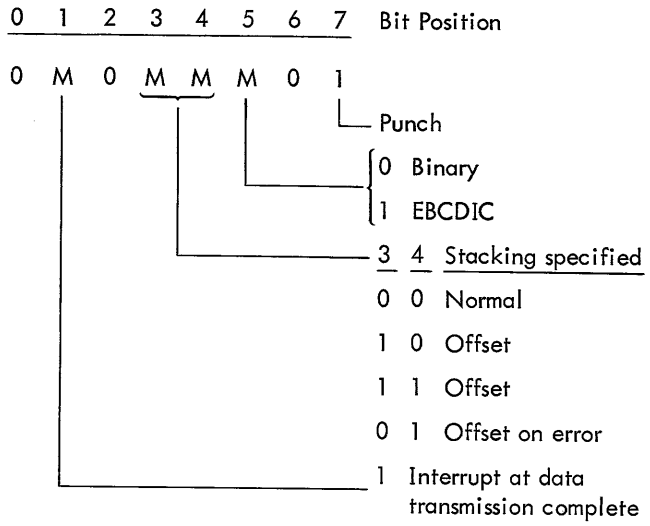
†Operator intervention is required when the hopper is empty, stacker is full, or chip box is full.

3. PROGRAM INTERFACE

PUNCH ORDERS

The 8-bit punch order specifies the binary or EBCDIC punch mode and whether normal or offset stacking is required. The specified punch mode applies to the entire card image; punch modes may not be changed for a given card. Cards proceed through the punch station one column at a time, column 1 first. In the EBCDIC mode, 1-byte service is requested per column. In the binary mode, 2-byte service is requested for all odd columns and 1-byte service for all even columns. In either mode, the image is transmitted once per card.

The following illustration indicates the required and optional bit configurations of the basic punch order. Bit positions 1 and 3-5 have indicated options. To be a valid order, bit 7 must be a "1".



PUNCH CARD EBCDIC

The following table lists the valid orders (hexadecimal code) to feed and punch a card in the EBCDIC mode.

Order	Action
X'05'	Stack card normally
X'45'[t]	Stack card normally
X'0D'	Offset stack on error
X'4D'[t]	Offset stack on error
X'15'	Offset stack
X'1D'	Offset stack
X'55'[t]	Offset stack
X'5D'[t]	Offset stack

[t]Interrupt at Data Transmission Complete (i.e., device-initiated interrupt occurs at zero byte count)

PUNCH CARD BINARY

The following table lists the valid orders (hexadecimal code) to feed and punch a card in the binary mode.

Order	Action
X'01'	Stack card normally
X'41'[t]	Stack card normally
X'09'	Offset stack on error
X'49'[t]	Offset stack on error
X'11'	Offset stack
X'19'	Offset stack
X'51'[t]	Offset stack
X'59'[t]	Offset stack

KEY EVENTS

The key events that occur during a card punch operation follow. No chronological order should be assumed from the order of presentation. Timing information is under "Programming Considerations".

START INPUT/OUTPUT

A card punch operation begins with the execution of a START INPUT/OUTPUT (SIO) instruction. If I/O address recognition exists and the punch is in the "ready" condition with no interrupt pending, the controlling system sets its "I/O address recognition" and "SIO accepted" indicators. The card punch advances from the "ready" to the "busy" condition, requests an order from the controlling system, and then waits for the order to arrive. In the manual mode, "SIO accepted" does not mean that the punch has started to feed and punch a card, only that it has acknowledged the I/O address and is in the "ready" condition with no interrupt pending.

UNUSUAL END CONDITIONS

Upon detecting any of the following conditions, after an order is received, the card punch returns an "unusual end" indication to the controlling system.

1. Invalid order code.
2. Transport mechanism malfunction (jam) while punching.
3. Power failure while punching.
4. RESET switch activated while punching.
5. Punch error (echo check).
6. Data overrun (rate error) while punching.

7. Access cover interlock opened while punching.
8. IOP halt during data transmission (not applicable to Sigma 2).
9. TEST switch (on maintenance panel) moved to TEST position while punching.
10. POWER switch pressed while punching.

CHANNEL END CONDITION

After receiving a valid order, the card punch signals "channel end" to the controlling system when a card being punched leaves the punch station or an "unusual end" condition occurs. A card may leave the punch station after punching any number of columns from 1 through 80, that is, after punching the byte preceding "count done".

FAULT CONDITIONS

A "fault" condition is any condition that causes a device to report a "not operational" condition in response to an SIO, HIO, or TIO instruction. The following conditions cause the card punch to become "not operational".

1. Transport mechanism malfunction (jam).
2. Interlock open.
3. TEST switch (on maintenance panel) in TEST position.
4. Absence of ac or dc power.
5. Pressing RESET switch.
6. Pressing POWER switch.

ERROR CONDITIONS

An error condition is any condition that results in invalid data being recorded, but does not cause the device to become "not operational"; thus, program recovery is possible. The card punch can detect and report the following error conditions to the controlling system:

Data Overrun (rate error). Data overrun will be reported if the data required for a given column is not received by "column advance" time. This will cause offset stacking if indicated by the order that caused this card feed. "Unusual end" will be reported at normal "channel end" time.

Punch Error (echo check). Punch error will be reported when the punch validation (echo check) circuitry detects a difference between the data punched and the data received. This error will cause offset stacking if indicated in the order that caused this card feed. "Unusual end" will be reported at normal "channel end" time.

Incorrect Length. Incorrect length will be reported if "count done" is not coincident with column 80 in either format. (This is not considered an error for stack on error.) It is valid to transmit fewer than 80 bytes in EBCDIC or 120 bytes in binary.

CARD PUNCH STATUS RESPONSE

The card punch can return status information in response to computer-executed I/O instructions. Detailed explanations of the I/O instructions are in the Sigma computer reference manuals.

I/O INSTRUCTION STATUS BITS

Execution of an I/O instruction provides two bits of information pertaining to the general status of the addressed I/O device and its controller. Table 3 lists the I/O instructions, status bit settings, and the significance of each setting.

DEVICE STATUS BYTE

Eight bits of information are made available to the controlling system in the Device Status Byte in response to the execution of an I/O instruction, as shown in Tables 4 and 5.

OPERATIONAL STATUS BYTE

In addition to the information contained in the Device Status Byte, the Operational Status Byte generated at the end of each I/O operation also provides indicators to the controlling system (see Table 6).

PROGRAMMING CONSIDERATIONS

Figure 4 illustrates card punch timing. Figure 5 illustrates the sequential relationship of the key events that occur during a card punch operation.

Table 3. Card Punch I/O Instruction Execution Response

Instruction	Status Bits†		Significance
	CC1 or O	CC2 or C	
SIO	0	0	I/O address recognized and SIO accepted.
	0	1	I/O address recognized but SIO not accepted.
	1	0	Selector IOP is "busy" (not applicable to Sigma 2).
	1	1	I/O address not recognized.

†The symbols CC1 and CC2 refer to condition code bits in Sigma 5/7 computers. The symbols O and C refer, respectively, to Overflow and Carry indicators in Sigma 2 computers.

Table 3. Card Punch I/O Instruction Execution Response (cont.)

Instruction	Status Bits† CC1 or O	CC2 or C	Significance
HIO	0	0	I/O address recognized and punch "not busy" when halt occurred.
	0	1	I/O address recognized and punch "busy" when halt occurred.
	1	0	Invalid code.
	1	1	I/O address not recognized.
TIO	0	0	I/O address recognized and SIO can currently be accepted.
	0	1	I/O address recognized but SIO cannot currently be accepted.
	1	0	Selector IOP is "busy" (not applicable to Sigma 2).
	1	1	I/O address not recognized.
TDV	0	0	I/O address recognized.
	0	1	I/O address recognized and subcontroller is in test mode.
	1	0	Selector IOP is "busy" (not applicable to Sigma 2).
	1	1	I/O address not recognized.
AIO	0	0	Normal interrupt condition present.
	0	1	Previous operation terminated in an "unusual end" condition.
	1	0	Invalid code.
	1	1	No interrupt condition present.

†The symbols CC1 and CC2 refer to condition code bits in Sigma 5/7 computers. The symbols O and C refer, respectively, to Overflow and Carry indicators in Sigma 2 computers.

Table 4. Device Status Response for SIO, TIO, and HIO

Bit Position	Function	State	Meaning
0	Device Interrupt Pending	1	Device interrupt is pending (issued, but not yet acknowledged by an AIO instruction). A new order will not be accepted until the interrupt is cleared by an AIO or HIO instruction, or manually (I/O reset from computer control panel).
1, 2	Card Punch Condition		A combination of these two bits indicates the current card punch condition:
		00	Card Punch Ready.
		01	Card Punch Not Operational. Manual intervention required to clear "not operational" condition.
		10	Device Unavailable – Not applicable.
		11	Card Punch Busy.
3	Mode-Automatic or Manual	0	Manual mode.
		1	Automatic mode.
4	Unusual End	1	Execution of previous punch order terminated due to abnormal condition, as listed under "Unusual End Conditions".
5, 6	Controller Condition		Same configurations as bits 1, 2.
7	Unassigned	0	Currently unassigned and always reset to zero.

Table 5. Device Status Response for TDV and AIO

Bit Position	Function	State	Meaning
0	Data Overrun	1	Data overrun (rate error) reported if data required for a given column not received by "column advance" time. This causes offset stacking if indicated by order that caused this card feed. "Unusual end" reported at "channel end".
1	Unassigned – TDV	0	Currently unassigned and always reset to zero.
	Data Transmission Complete Interrupt – AIO	1	Data Transmission Complete interrupt occurred.
2	Punch Error	1	Punch error reported when punch validation (echo check) circuitry detects difference between data punched and data received. This error causes offset stacking if indicated in the order that caused this card feed. "Unusual end" is reported at "channel end".
3–7	Unassigned	0	Currently unassigned and always reset to zeros.

Table 6. Operational Status Byte[†]

Bit Position	Function	State	Meaning
0	Transmission Data Error (data overrun)	1	See Table 5, Bit Position 0.
1	Incorrect Length	1	Byte counts are 80 for EBCDIC and 120 for binary. If any other count used, incorrect length reported at channel end. If less than these counts used, card rate is increased as shown in Figure 1. If more than these counts are used, punching is terminated with column 80.
2	Chaining Modifier	0	Not used and always reset to zero.
3	Channel End	1	I/O operations have been terminated for any reason listed under "Channel End Conditions".
4	Unusual End	1	Execution of previous order terminated due to abnormal condition (see "Unusual End Conditions").
5–7	Unassigned	0	Currently unassigned and always reset to zero.

[†]For Sigma 2 computers. For Sigma 5/7 computers, see the "Operational Status Byte" in the applicable computer reference manual.

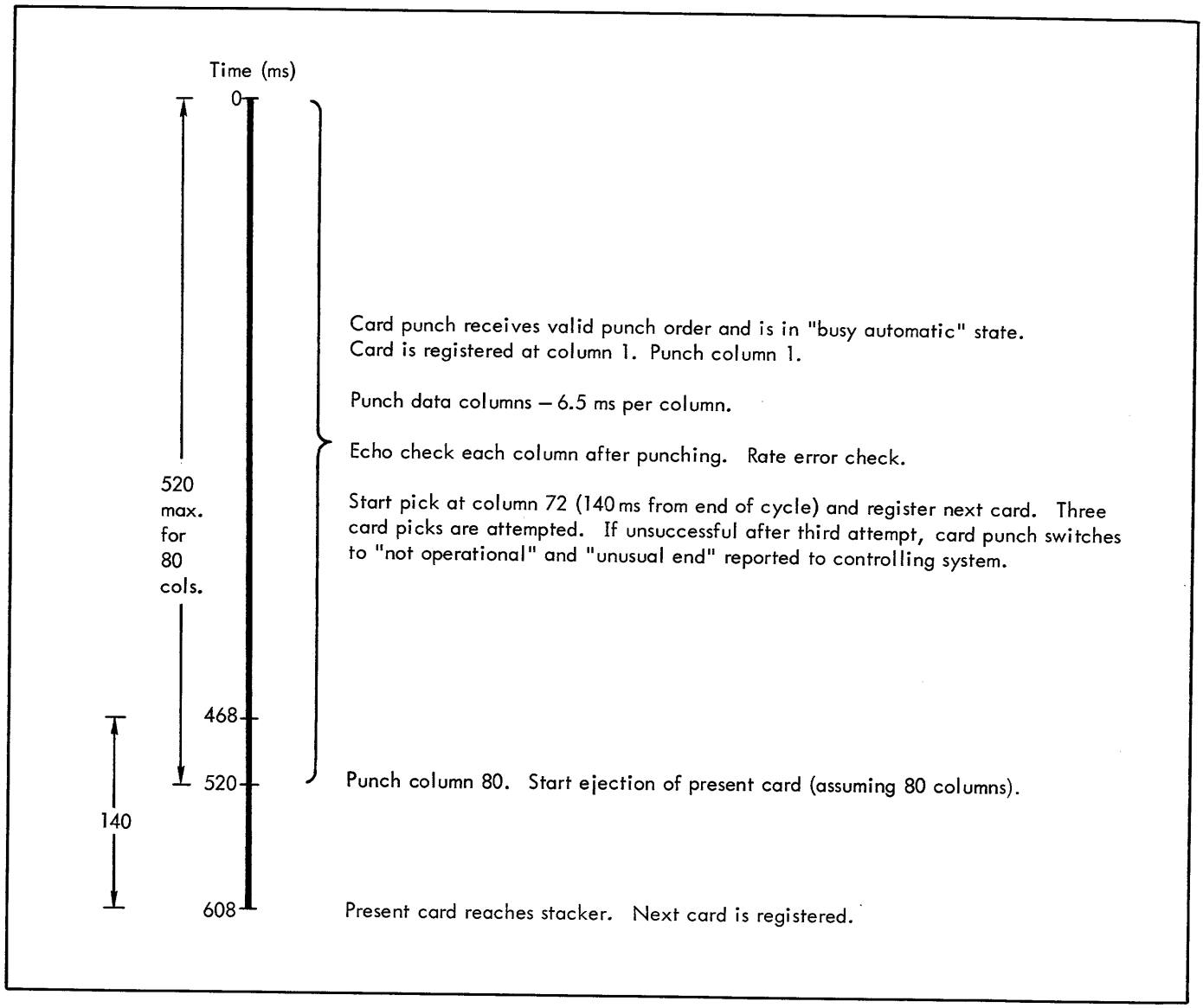
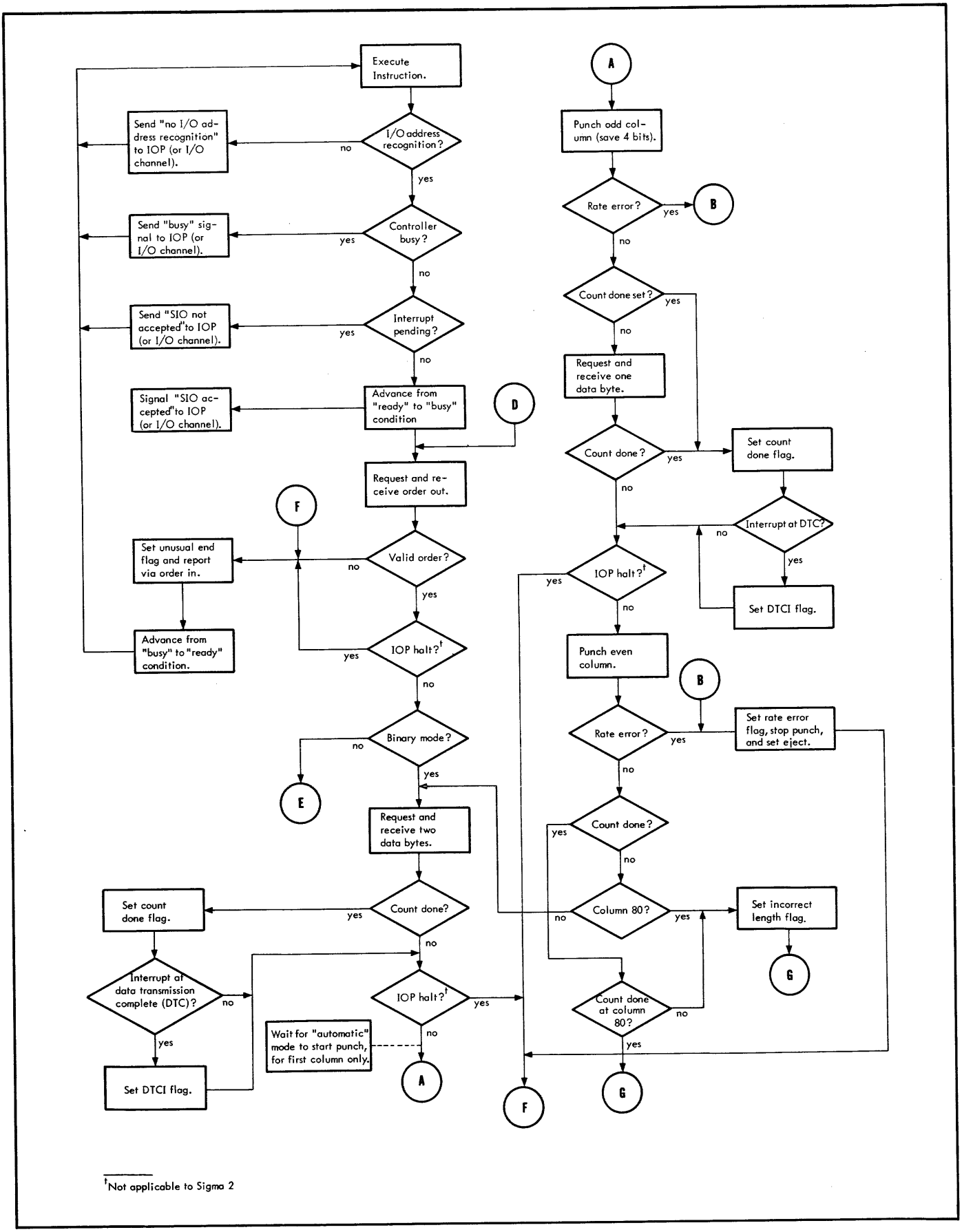


Figure 4. Card Punch Timing



†Not applicable to Sigma 2

Figure 5. Controlling System and Card Punch Actions

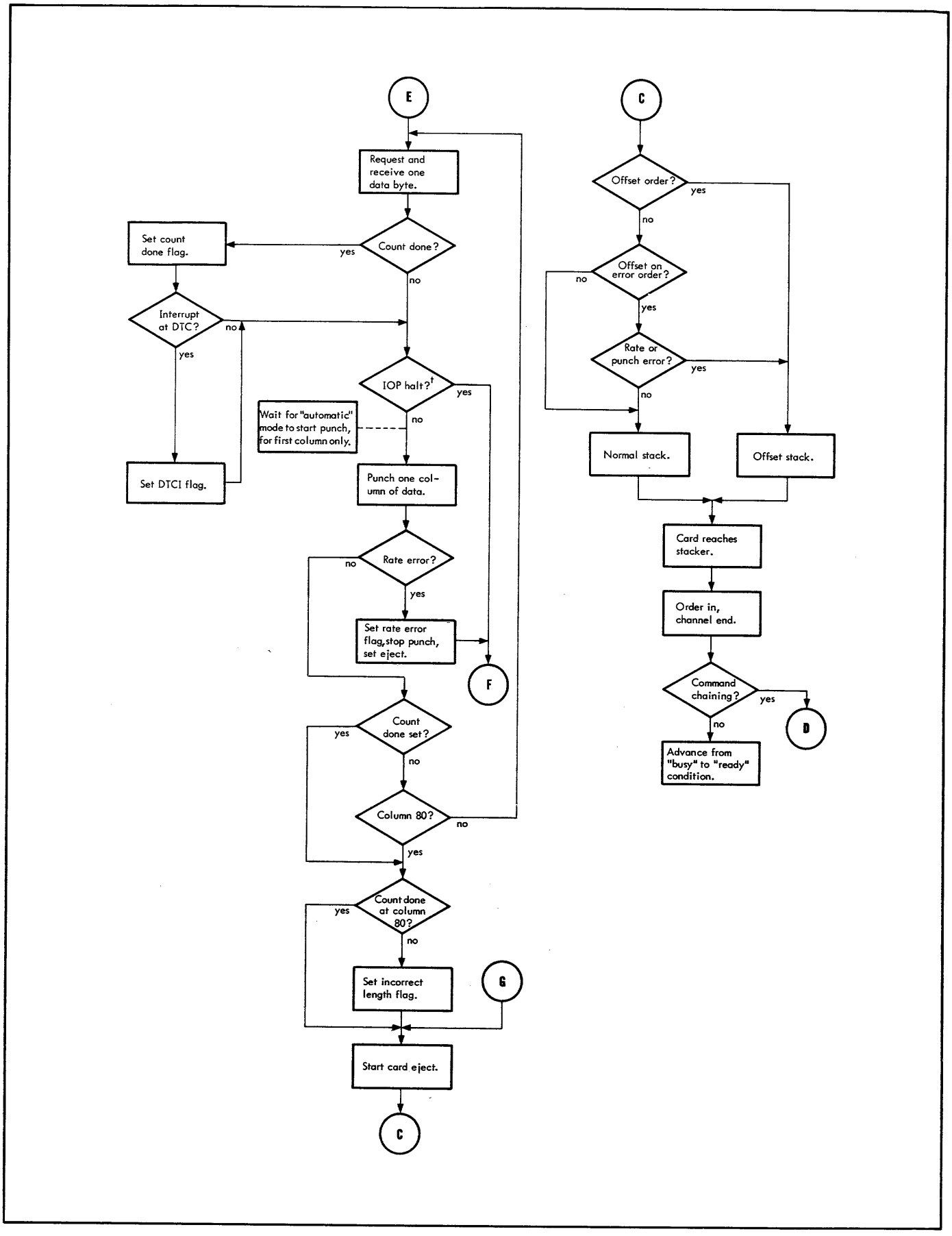


Figure 5. Controlling System and Card Punch Actions (cont.)

4. OPERATIONS

OPERATOR CONTROLS

The control panel, which is located in the access (top) cover, contains eight switches and indicators (see Figures 6 and 7).

POWER

This push-on/push-off switch-indicator controls ac power to the card punch motor. The switch does not control dc power to the punch unit. The indicator is illuminated when the switch is on.

START

When this switch-indicator is activated, the punch enters the automatic mode provided that it is operational and operator intervention is not required. The indicator is illuminated when the punch is in the automatic mode. The card punch is "operational" if the following conditions are satisfied.

1. Power is applied.
2. Cover interlock is closed.
3. Transport fault not present.

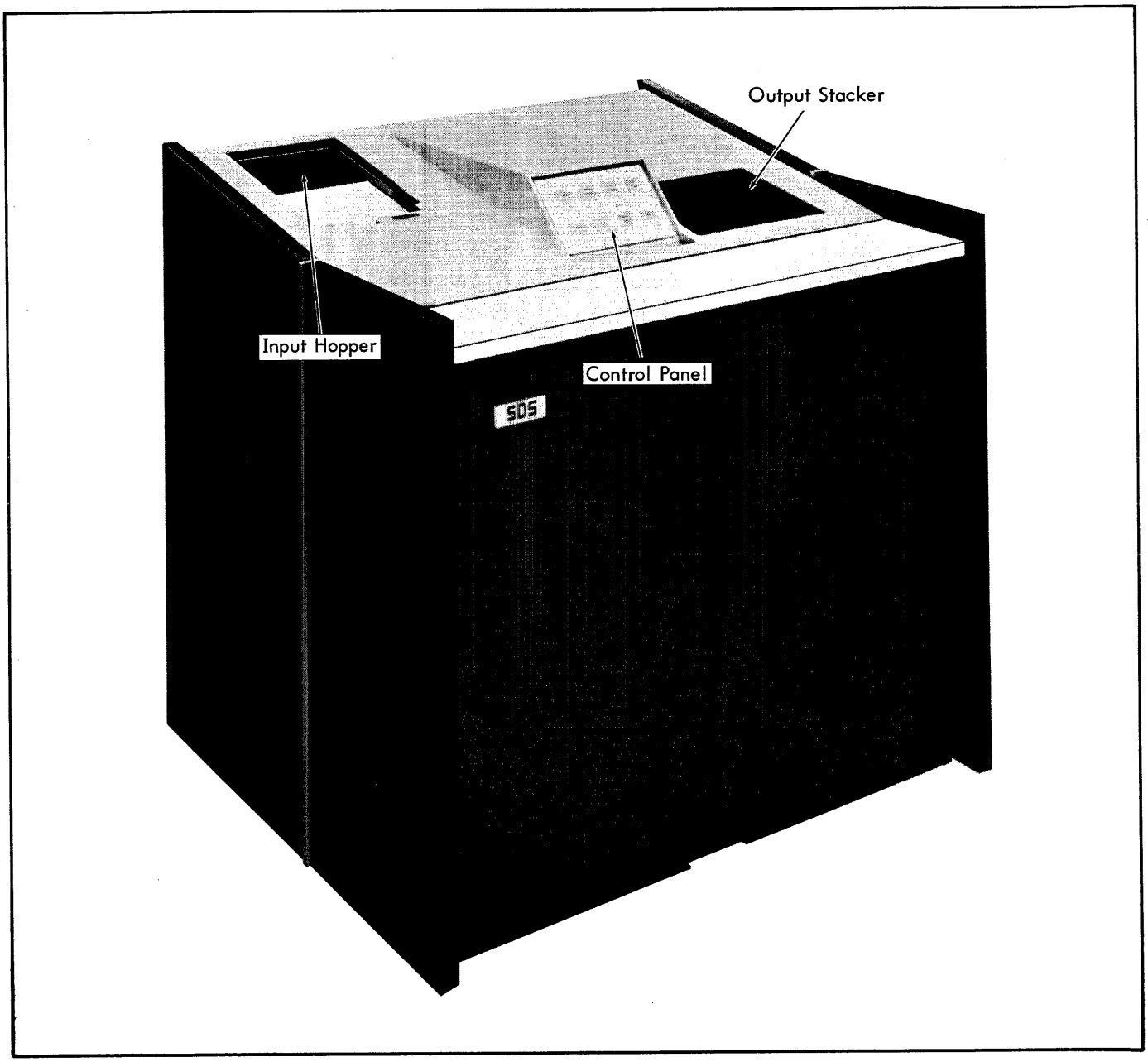


Figure 6. Model 7165 Card Punch

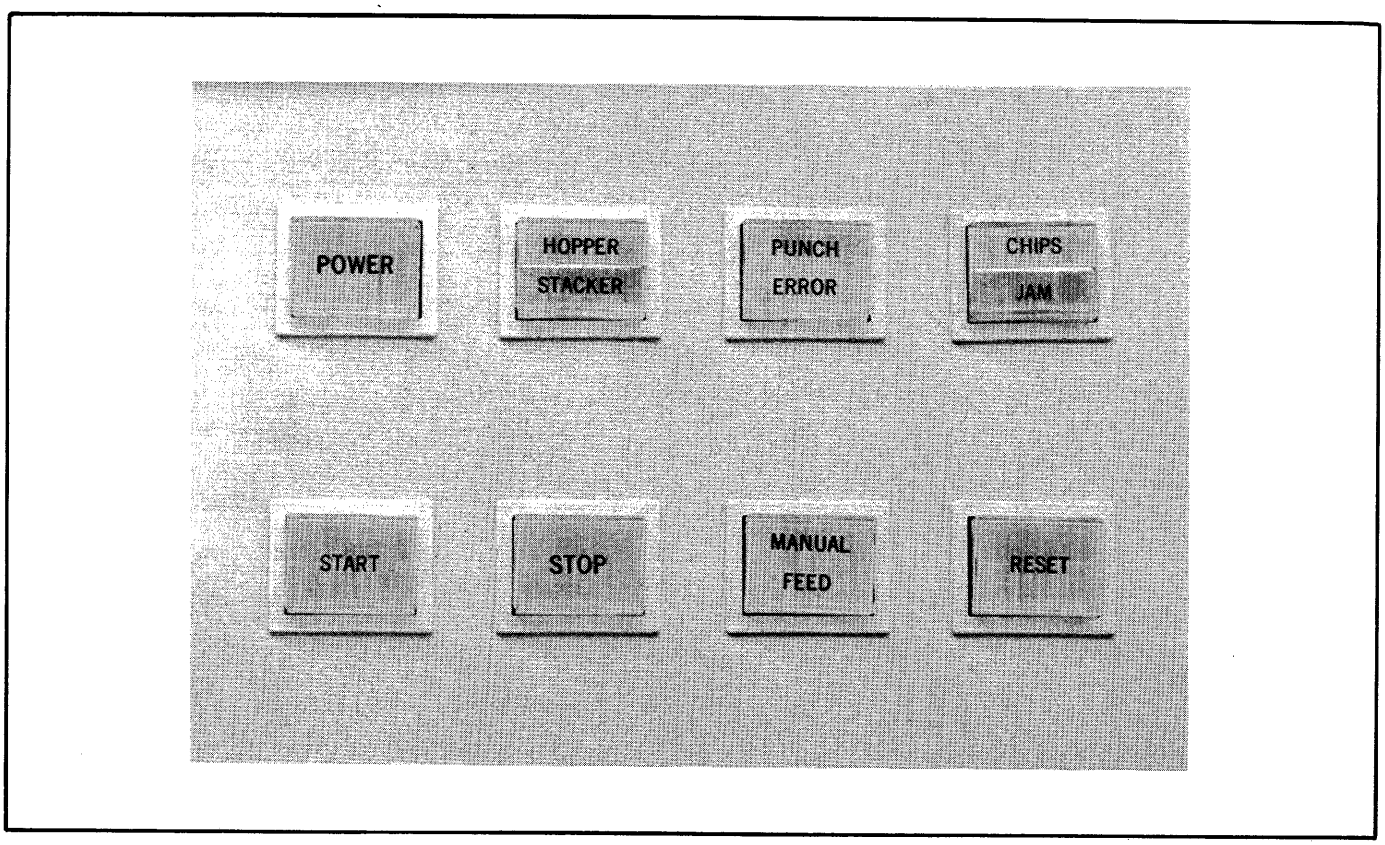


Figure 7. Control Panel

4. RESET switch on control panel not activated.

5. TEST switch (on maintenance panel) is off.

Operator intervention is required if

1. Hopper is empty.

2. Stacker is full.

3. Chip box is full or out of place.

4. Manual feed is required.

   Note: Pressing the START switch when manual feed is required causes the MANUAL FEED indicator to illuminate.

STOP

When this switch-indicator is activated, the punch completes the operation on the card being processed before stopping and entering the manual mode. The indicator is illuminated when the punch is in the manual mode.

MANUAL FEED

Activating this switch-indicator causes a single card-feed cycle to occur provided that the punch is in the manual mode and all current card cycles are completed. A card-feed cycle is as follows:

1. If a card is present in the punch station, it is transported to the output stacker.

2. If the hopper is not empty, a card is picked and transported to the punch station and registered for punching.

The indicator is illuminated while the switch is activated.

RESET

Activating this switch-indicator clears the punch error and jam indicators. If the punch is "busy", an "unusual end" condition will be reported. The indicator is illuminated while the switch is activated.

If the RESET switch is pressed during any program-controlled operation, the program must be restarted since all punch data will have been eradicated.

HOPPER/STACKER

The HOPPER portion of this split-field indicator illuminates when the hopper becomes empty. The HOPPER field remains on until the operator places cards in the hopper and activates the START or MANUAL FEED switch.

The STACKER field illuminates when the stacker becomes full; it remains on until the operator removes cards from the stacker and activates the START or MANUAL FEED switch.

PUNCH ERROR

This indicator illuminates when a punch error is detected. It remains on until the START, MANUAL FEED, or RESET switch is activated.

CHIPS/JAM

The CHIPS field of this split-field indicator illuminates when the chip box is full or not properly in place. It remains on until the operator properly replaces the empty chip box and activates the START or MANUAL FEED switch. (The chip box is located behind the left front door.)

The JAM field illuminates when a transport fault is detected. After the fault is remedied, the operator presses the RESET switch to turn off the indicator. Transport faults are defined as:

1. A pick failure, occurring when three attempts to pick and deliver a card into the transport have been made without success.
2. A registration failure, occurring when a picked card fails to register at the punch station.
3. A punch station exit failure, occurring when a card fails to exit the punch station or is not delivered to the stacker.

Note: The motor is shut off immediately if a transport fault (jam) is detected.

INPUT HOPPER

The input hopper (see Figure 6) is located on the left side of the upper cabinet. Its capacity is 1000 cards. The wheeled card weight rests against cards in the hopper. Since the bed of the hopper is inclined toward the picker assembly, cards are gravity fed to the pick roller. A switch senses when the hopper is empty.

OUTPUT STACKER

The output stacker (see Figure 6) is located at the right side of the cabinet. Its capacity is 1000 cards. Cards enter the stacker aided by the output stacker rollers. The spring-loaded follower plate maintains the cards in proper position. A switch (actuated by the follower plate) senses when the stacker is full.

Associated with the stacker is an offset assembly that raises a selected card approximately one-half inch upon command. This feature is used for identifying error cards or separating decks. It must not be used continuously for large groups of cards; otherwise, card damage will occur.

COVER INTERLOCK

An interlock switch, located under the top cover, is closed when the cover is in place. When the cover is raised, the spring-loaded switch opens and disables the punch.

OPERATING INSTRUCTIONS

This section describes operating, turn-on, halt, and jam-clearing procedures.

OPERATING PREPARATION

Before operating the card punch, use the following procedures:

1. Check the hopper and stacker to see that they are free of foreign matter.
2. Check the chip box.
3. Prepare the cards for use by ruffling and flexing them. Tamp the cards so that the deck is square.
4. Inspect edges of cards for irregularities.
5. With nine-edge up and column one to the right, place cards in the hopper. Put the card weight against the cards.

TURN-ON PROCEDURE

1. Press the POWER switch on the control panel. The POWER and STOP indicators will illuminate.
2. Press the MANUAL FEED switch. The MANUAL FEED indicator will illuminate. One card will be transported to the registration station.
3. Press the START switch. The START indicator will illuminate.

The card punch is now ready for operation under program control.

CONTINUOUS OPERATION

The card punch may be operated continuously provided that the operator adheres to the following practices:

1. Do not remove card weight from the cards in the hopper when there are less than three inches of cards remaining (this may cause a jam).
2. Add cards to hopper before the card deck is less than three inches high.
3. Remove cards from stacker before it is full.

MOMENTARY HALT

The following procedure enables the operator to interrupt the operation of the card punch and restart it at the point of interruption.

1. Press the STOP switch.
2. Perform the required task.
3. Press the START switch.

AUTOMATIC RECOVERABLE HALT

The following conditions cause the punch to enter the "manual" mode. Performing the required task and pressing the START switch will restart the punch with no loss of information.

1. Hopper empty
2. Stacker full
3. Chip box full

CLEARING CARD JAMS

When a transport jam is sensed, the JAM field of the CHIPS/JAM indicator on the control panel will illuminate. Also, the appropriate FAULT INDICATOR on the maintenance panel (inside the right front door) will illuminate. In case of repeated failures, call Customer Engineering maintenance personnel. The procedures for clearing card jams are outlined below (see Figures 8 and 9).

Note: Be careful in clearing a card jam to avoid damage to the mechanism.

PICK JAM

1. Remove cards from input hopper and transport mechanism.
2. Check leading edges of cards for irregularities. Remove damaged cards.
3. Ruffle and flex the card deck. Tamp the cards so that the deck is square. Replace cards in hopper.
4. Press RESET switch to clear all indicators and then resume operation.

THROAT JAM

1. Remove cards from input hopper and transport mechanism.
2. Open registration station by lifting hinged cover catch and pressing it (toward rear of unit).
3. Turn hand wheel until the jammed card can be removed. Remove all pieces of the card.
4. Close registration station.
5. Replace cards in hopper.
6. Press RESET switch to clear all indicators and then resume operation.

REGISTRATION JAM

1. Press RESET switch and then MANUAL FEED switch. This may eject the irregular card.
2. If step 1 is unsuccessful, open registration station.
3. Apply thumb pressure (toward back of machine) to the feed wheel lever on the punch head to disengage pressure roller from feed wheel. Remove card.
4. Close registration station.
5. Press RESET switch to clear all indicators and then resume operation.

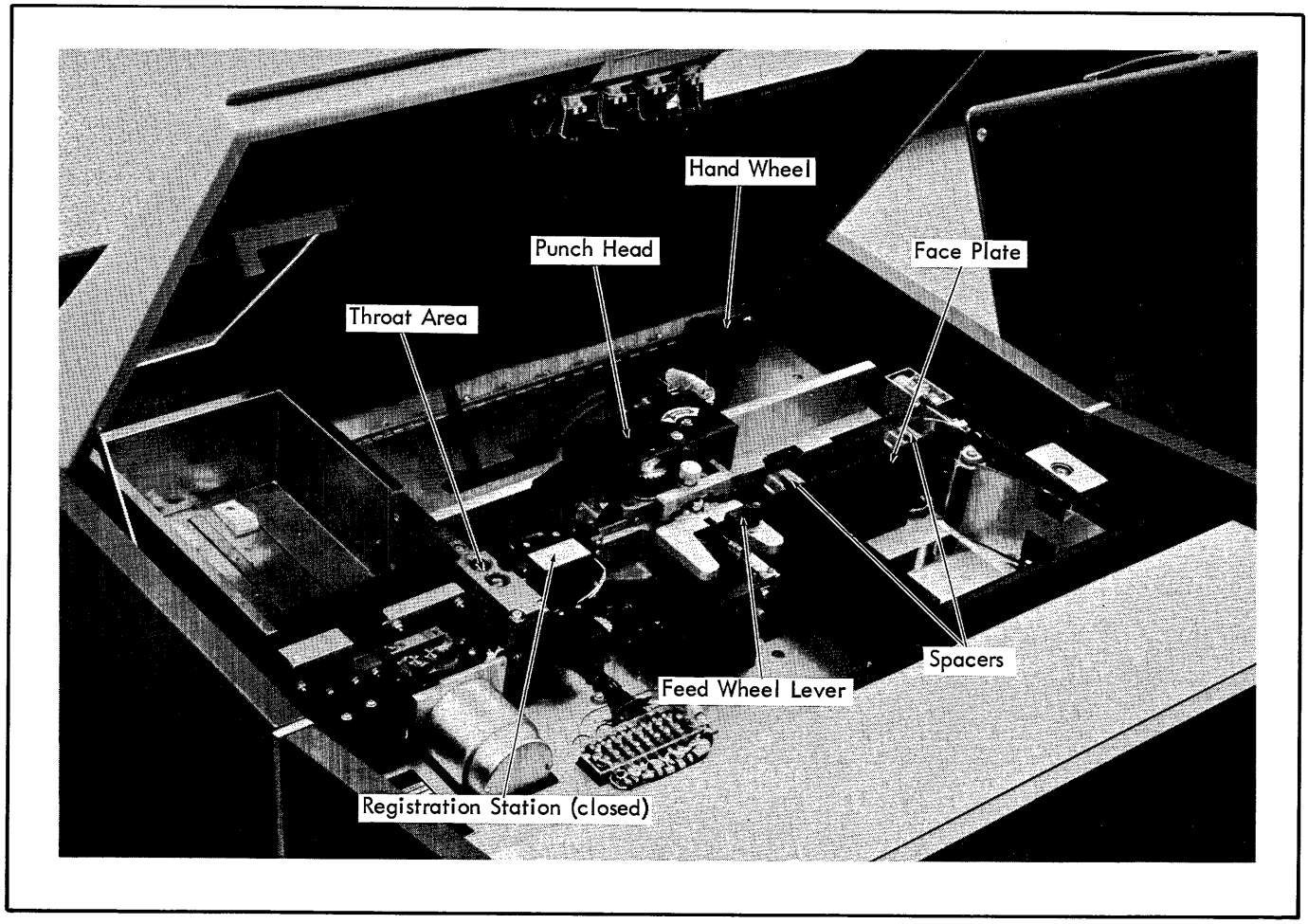


Figure 8. Card Punch Mechanism with Access Cover Open

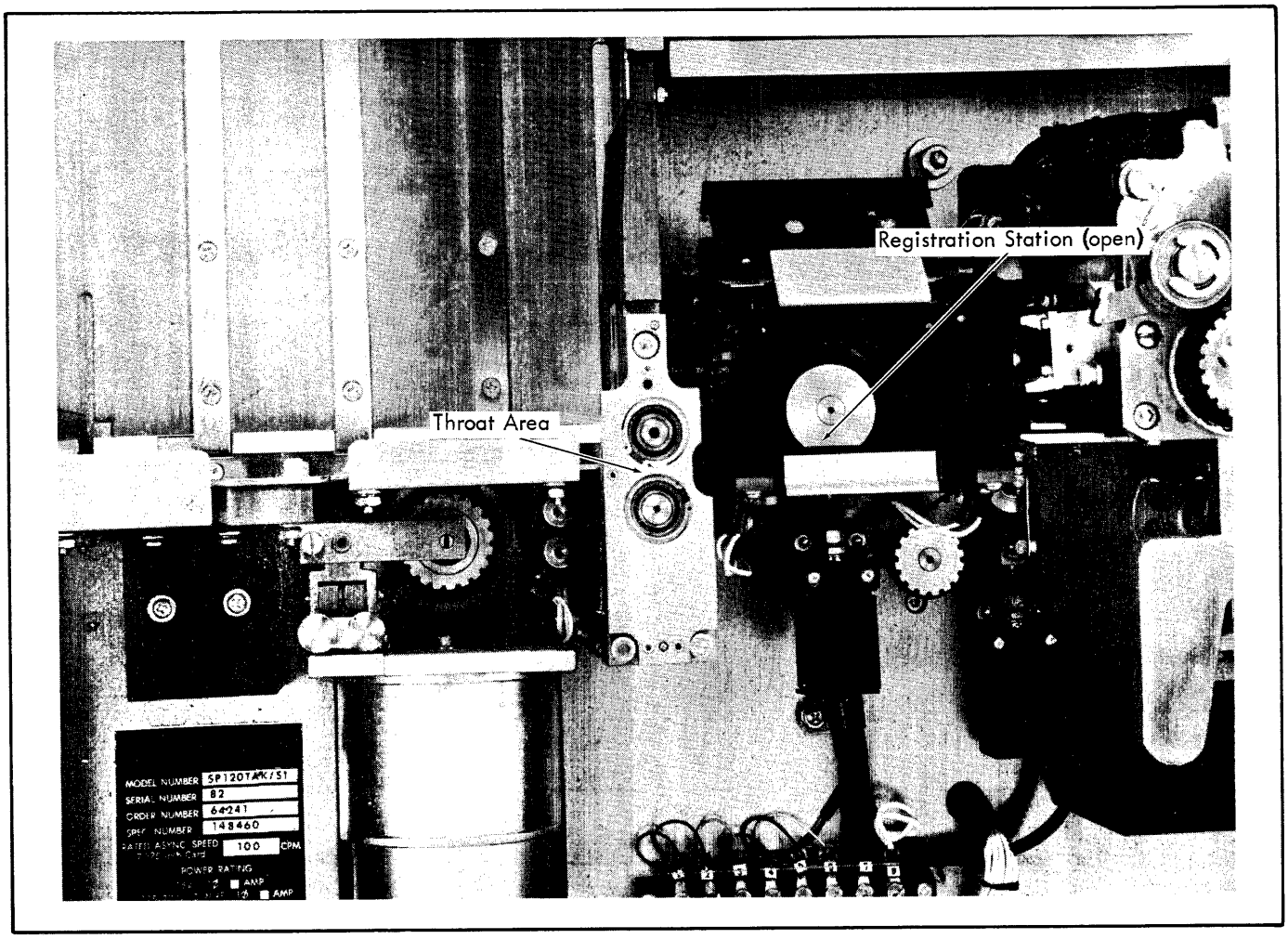


Figure 9. Card Punch Mechanism, Left View

EJECT JAM

1. Remove face plate by placing fingers under the clear plastic spacers and lifting up.

   Note: If jammed card is in stacker area, it is unnecessary to remove face plate.

2. Turn the hand wheel until the jammed card can be removed.

3. Replace face plate carefully, ensuring that no damage occurs to the alignment pins.

4. Press RESET switch to clear all indicators and then resume operation.

PUNCH HEAD JAM

If the card jam is in the punch head area, do not attempt to clear the jam. Call Customer Engineering maintenance personnel.

APPENDIX A. SDS STANDARD SYMBOLS, CODES, AND CORRESPONDENCES

This appendix contains the following reference material:

Title

SDS Standard Symbols and Codes

Standard 8-Bit Computer Codes (EBCDIC - Extended Binary-Coded-Decimal Interchange Code)

SDS Standard 7-Bit Communication Codes (USASCII - United States of America Standard Code for Information Interchange)

SDS Standard Symbol-Code Correspondences

SDS STANDARD SYMBOLS AND CODES

The symbol and code standards described in this publication are applicable to all SDS products, both hardware and software. They may be expanded or altered from time to time to meet changing requirements.

The symbols listed here include two types: graphic symbols and control characters. Graphic symbols are displayable and printable; control characters are not. Hybrids are SP (the symbol for a blank space), and DEL (the delete code) which is not considered a control command.

Three types of code are shown: (1) the 8-bit SDS Standard Computer Code, i.e., the SDS Extended Binary-Coded-Decimal Interchange Code (EBCDIC); (2) the 7-bit United States of America Standard Code for Information Interchange (USASCII); and (3) correspondence between these two codes.

SDS STANDARD CHARACTER SETS

1. EBCDIC

   57-character set: uppercase letters, numerals, space, and & - / . < > ( ) + | $ * : ; , % # @ ' =

   63-character set: Same as above plus ¢ ! _ ? " ¬

   89-character set: same as 63-character set plus lowercase letters

2. USASCII

   64-character set: uppercase letters, numerals, space, and ! " $ % & ' ( ) * + , - . / \ ; : = < > ? @ _ [ ] ^ #

   95-character set: same as above plus lowercase letters and { } ¦ ~ `

CONTROL CODES

In addition to the standard character sets listed above, the SDS symbol repertoire includes 37 control codes and the hybrid code DEL (hybrid code SP is considered part of all character sets). These are listed in the table titled SDS Standard Symbol-Code Correspondences.

SPECIAL CODE PROPERTIES

The following two properties of all SDS standard codes will be retained for future standard code extensions:

1. All control codes, and only the control codes, have their two high-order bits equal to "00". DEL is not considered a control code.

2. No two graphic EBCDIC codes have their seven low-order bits equal.

SDS STANDARD 8-BIT COMPUTER CODES (EBCDIC)

Least Significant Digits		Most Significant Digits: 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Hexadecimal																	
	Binary	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0	0000	NUL	DLE	ds		SP	&	-									0
1	0001	SOH	DC1	ss				/		a	j		\[1]	A	J		1
2	0010	STX	DC2	fs						b	k	s	{[1]	B	K	S	2
3	0011	ETX	DC3	si						c	l	t	}[1]	C	L	T	3
4	0100	EOT	DC4							d	m	u	[[1]	D	M	U	4
5	0101	HT	LF NL			Will not be assigned				e	n	v	][1]	E	N	V	5
6	0110	ACK	SYN							f	o	w		F	O	W	6
7	0111	BEL	ETB							g	p	x		G	P	X	7
8	1000	EOM BS	CAN							h	q	y		H	Q	Y	8
9	1001	ENQ	EM							i	r	z		I	R	Z	9
A	1010	NAK	SS			¢[2]	!	~[1]	:								
B	1011	VT	ESC			.	$	,	#								
C	1100	FF	FS			<	*	%	@					Will not be assigned			
D	1101	CR	GS			(	)	_	'								
E	1110	SO	RS			+	;	>	=								
F	1111	SI	US	PE		|[2]	¬[2]	?	"								DEL
		3				4				5							

NOTES:

1 The characters ^ \ { } [ ] are USASCII characters that do not appear in any of the SDS EBCDIC-based character sets, though they are shown in the EBCDIC table.

2 The characters ¢ | ¬ appear in the SDS 63- and 89-character EBCDIC sets but not in either of the SDS USASCII-based sets, However, SDS software translates the characters ¢ | ¬ into USASCII characters as follows:

EBCDIC	=	UASCII
¢		` (6-0)
|		¦ (7-12)
¬		~ (7-14)

3 The EBCDIC control codes in columns 0 and 1 and their binary representation are exactly the same as those in the USASCII table, except for two interchanges: LF/NL with NAK, and HT with ENQ.

4 Characters enclosed in heavy lines are included only in the SDS standard 63- and 89-character EBCDIC sets.

5 These characters are included only in the SDS standard 89-character EBCDIC set.

SDS STANDARD 7-BIT COMMUNICATION CODES (USASCII)[1]

Least Significant Digits		Most Significant Digits: 0	1	2	3	4	5	6	7
Decimal (rows) (col's.)									
	Binary[1]	x000	x001	x010	x011	x100	x101	x110	x111
0	0000	NUL	DLE	SP	0	@	P	`	p
1	0001	SOH	DC1	!5	1	A	Q	a	q
2	0010	STX	DC2	"	2	B	R	b	r
3	0011	ETX	DC3	#	3	C	S	c	s
4	0100	EOT	DC4	$	4	D	T	d	t
5	0101	ENQ	NAK	%	5	E	U	e	u
6	0110	ACK	SYN	&	6	F	V	f	v
7	0111	BEL	ETB	'	7	G	W	g	w
8	1000	BS	CAN	(	8	H	X	h	x
9	1001	HT	EM	)	9	I	Y	i	y
10	1010	LF NL	SS	*	:	J	Z	j	z
11	1011	VT	ESC	+	;	K	[5	k	{
12	1100	FF	FS	,	<	L	\	l	¦
13	1101	CR	GS	-	=	M	]5	m	}
14	1110	SO	RS	.	>	N	4^5	n	~4
15	1111	SI	US	/	?	O	_4	o	DEL
		2				3			

NOTES:

1 Most significant bit, added for 8-bit format, is either 0 or an odd-parity bit for the remaining 7 bits.

2 Columns 0-1 are control codes.

3 Columns 2-5 correspond to the SDS 64-character USASCII set.
Columns 2-7 correspond to the SDS 95-character USASCII set.

4 On many current teletypes, the symbol

^ is ↑ (5-14)
_ is ← (5-15)
~ is ESC or ALTMODE control (7-14)

and none of the symbols appearing in columns 6-7 are provided. Except for the three symbol differences noted above, therefore, such teletypes provide all the characters in the SDS 64-character USASCII set. (The SDS 7015 Remote Keyboard Printer provides the 64-character USASCII set also, but prints ^ as ∧.)

5 On the SDS 7670 Remote Batch Terminal, the symbol

! is | (2-1)
[is ¢ (5-11)
] is ! (5-13)
^ is ¬ (5-14)

and none of the symbols appearing in columns 6-7 are provided. Except for the four symbol differences noted above, therefore, this terminal provides all the characters in the SDS 64-character USASCII set.

SDS STANDARD SYMBOL-CODE CORRESPONDENCES

EBCDIC[t]	Symbol	Card Code	USASCII[tt]	Meaning	Remarks
00	NUL	12-0-9-8-1	0-0	null	00 through 23 and 2F are control codes.
01	SOH	12-9-1	0-1	start of header	
02	STX	12-9-2	0-2	start of text	
03	ETX	12-9-3	0-3	end of text	
04	EOT	12-9-4	0-4	end of transmission	
05	HT	12-9-5	0-9	horizontal tab	
06	ACK	12-9-6	0-6	acknowledge (positive)	
07	BEL	12-9-7	0-7	bell	
08	BS or EOM	12-9-8	0-8	backspace or end of message	EOM is used only on SDS Keyboard/ Printers Models 7012, 7020, 8091, and 8092.
09	ENQ	12-9-8-1	0-5	enquiry	
0A	NAK	12-9-8-2	1-5	negative acknowledge	
0B	VT	12-9-8-3	0-11	vertical tab	
0C	FF	12-9-8-4	0-12	form feed	
0D	CR	12-9-8-5	0-13	carriage return	
0E	SO	12-9-8-6	0-14	shift out	
0F	SI	12-9-8-7	0-15	shift in	
10	DLE	12-11-9-8-1	1-0	data link escape	
11	DC1	11-9-1	1-1	device control 1	
12	DC2	11-9-2	1-2	device control 2	
13	DC3	11-9-3	1-3	device control 3	
14	DC4	11-9-4	1-4	device control 4	
15	LF or NL	11-9-5	0-10	line feed or new line	
16	SYN	11-9-6	1-6	sync	
17	ETB	11-9-7	1-7	end of transmission block	
18	CAN	11-9-8	1-8	cancel	
19	EM	11-9-8-1	1-9	end of medium	
1A	SS	11-9-8-2	1-10	start of special sequence	
1B	ESC	11-9-8-3	1-11	escape	
1C	FS	11-9-8-4	1-12	file separator	
1D	GS	11-9-8-5	1-13	group separator	
1E	RS	11-9-8-6	1-14	record separator	
1F	US	11-9-8-7	1-15	unit separator	
20	ds	11-0-9-8-1		digit selector	20 through 23 are used with Sigma 7 EDIT BYTE STRING (EBS) instruction — not input/output control codes.
21	ss	0-9-1		significance start	
22	fs	0-9-2		field separation	
23	si	0-9-3		immediate significance start	
24		0-9-4			24 through 2E are unassigned.
25		0-9-5			
26		0-9-6			
27		0-9-7			
28		0-9-8			
29		0-9-8-1			
2A		0-9-8-2			
2B		0-9-8-3			
2C		0-9-8-4			
2D		0-9-8-5			
2E		0-9-8-6			
2F	PE	0-9-8-7		parity error	If parity checking is requested.
30		12-11-0-9-8-1			30 through 3F are unassigned.
31		9-1			
32		9-2			
33		9-3			
34		9-4			
35		9-5			
36		9-6			
37		9-7			
38		9-8			
39		9-8-1			
3A		9-8-2			
3B		9-8-3			
3C		9-8-4			
3D		9-8-5			
3E		9-8-6			
3F		9-8-7			

[t]Hexadecimal notation.

[tt]Decimal notation (column-row).

SDS Standard Symbol-Code Correspondences (cont.)

EBCDIC†	Symbol	Card Code	USASCII††	Meaning	Remarks
40	SP	blank	2-0	blank	
41		12-0-9-1			41 through 49 will not be assigned.
42		12-0-9-2			
43		12-0-9-3			
44		12-0-9-4			
45		12-0-9-5			
46		12-0-9-6			
47		12-0-9-7			
48		12-0-9-8			
49		12-8-1			
4A	¢ or `	12-8-2	6-0	cent or accent grave	Accent grave used for left single quote. On model 7670, ` not available, and ¢ = USASCII 5-11.
4B	.	12-8-3	2-14	period	
4C	<	12-8-4	3-12	less than	
4D	(	12-8-5	2-8	left parenthesis	
4E	+	12-8-6	2-11	plus	
4F	| or ¦	12-8-7	7-12	vertical bar or broken bar	On Model 7670, ¦ not available, and | = ASASCII 2-1.
50	&	12	2-6	ampersand	
51		12-11-9-1			51 through 59 will not be assigned.
52		12-11-9-2			
53		12-11-9-3			
54		12-11-9-4			
55		12-11-9-5			
56		12-11-9-6			
57		12-11-9-7			
58		12-11-9-8			
59		11-8-1			
5A	!	11-8-2	2-1	exclamation point	On Model 7670, ! is |.
5B	$	11-8-3	2-4	dollars	
5C	*	11-8-4	2-10	asterisk	
5D	)	11-8-5	2-9	right parenthesis	
5E	;	11-8-6	3-11	semicolon	
5F	~ or ¬	11-8-7	7-14	tilde or logical not	On Model 7670, ~ is not available, and ¬ = USASCII 5-14.
60	-	11	2-13	minus, dash, hyphen	
61	/	0-1	2-15	slash	
62		11-0-9-2			62 through 69 will not be assigned.
63		11-0-9-3			
64		11-0-9-4			
65		11-0-9-5			
66		11-0-9-6			
67		11-0-9-7			
68		11-0-9-8			
69		0-8-1			
6A	^	12-11	5-14	circumflex	On Model 7670 ^ is ¬. On Model 7015 ^ is ∧ (caret).
6B	,	0-8-3	2-12	comma	
6C	%	0-8-4	2-5	percent	
6D	_	0-8-5	5-15	underline	Underline is sometimes called "break character"; may be printed along bottom of character line.
6E	>	0-8-6	3-14	greater than	
6F	?	0-8-7	3-15	question mark	
70		12-11-0			70 through 79 will not be assigned.
71		12-11-0-9-1			
72		12-11-0-9-2			
73		12-11-0-9-3			
74		12-11-0-9-4			
75		12-11-0-9-5			
76		12-11-0-9-6			
77		12-11-0-9-7			
78		12-11-0-9-8			
79		8-1			
7A	:	8-2	3-10	colon	
7B	#	8-3	2-3	number	
7C	@	8-4	4-0	at	
7D	'	8-5	2-7	apostrophe (right single quote)	
7E	=	8-6	3-13	equals	
7F	"	8-7	2-2	quotation mark	

†Hexadecimal notation

††Decimal notation (column-row).

SDS Standard Symbol-Code Correspondences (cont.)

EBCDIC†	Symbol	Card Code	USASCII††	Meaning	Remarks
80		12-0-8-1			80 is unassigned.
81	a	12-0-1	6-1		81-89, 91-99, A2-A9 comprise the lowercase alphabet. Available only in SDS standard 89- and 95-character sets.
82	b	12-0-2	6-2		
83	c	12-0-3	6-3		
84	d	12-0-4	6-4		
85	e	12-0-5	6-5		
86	f	12-0-6	6-6		
87	g	12-0-7	6-7		
88	h	12-0-8	6-8		
89	i	12-0-9	6-9		
8A		12-0-8-2			8A through 90 are unassigned.
8B		12-0-8-3			
8C		12-0-8-4			
8D		12-0-8-5			
8E		12-0-8-6			
8F		12-0-8-7			
90		12-11-8-1			
91	j	12-11-1	6-10		
92	k	12-11-2	6-11		
93	l	12-11-3	6-12		
94	m	12-11-4	6-13		
95	n	12-11-5	6-14		
96	o	12-11-6	6-15		
97	p	12-11-7	7-0		
98	q	12-11-8	7-1		
99	r	12-11-9	7-2		
9A		12-11-8-2			9A through A1 are unassigned.
9B		12-11-8-3			
9C		12-11-8-4			
9D		12-11-8-5			
9E		12-11-8-6			
9F		12-11-8-7			
A0		11-0-8-1			
A1		11-0-1			
A2	s	11-0-2	7-3		
A3	t	11-0-3	7-4		
A4	u	11-0-4	7-5		
A5	v	11-0-5	7-6		
A6	w	11-0-6	7-7		
A7	x	11-0-7	7-8		
A8	y	11-0-8	7-9		
A9	z	11-0-9	7-10		
AA		11-0-8-2			AA through B0 are unassigned.
AB		11-0-8-3			
AC		11-0-8-4			
AD		11-0-8-5			
AE		11-0-8-6			
AF		11-0-8-7			
B0		12-11-0-8-1			
B1	\	12-11-0-1	5-12	backslash	
B2	{	12-11-0-2	7-11	left brace	
B3	}	12-11-0-3	7-13	right brace	
B4	[	12-11-0-4	5-11	left bracket	On Model 7670, [is ¢.
B5	]	12-11-0-5	5-13	right bracket	On Model 7670,] is !.
B6		12-11-0-6			B6 through BF are unassigned.
B7		12-11-0-7			
B8		12-11-0-8			
B9		12-11-0-9			
BA		12-11-0-8-2			
BB		12-11-0-8-3			
BC		12-11-0-8-4			
BD		12-11-0-8-5			
BE		12-11-0-8-6			
BF		12-11-0-8-7			

†Hexadecimal notation.

††Decimal notation (column-row).

SDS Standard Symbol-Code Correspondences (cont.)

EBCDIC†	Symbol	Card Code	USASCII††	Meaning	Remarks
C0		12-0			C0 is unassigned.
C1	A	12-1	4-1		C1-C9, D1-D9, E2-E9 comprise the uppercase alphabet.
C2	B	12-2	4-2		
C3	C	12-3	4-3		
C4	D	12-4	4-4		
C5	E	12-5	4-5		
C6	F	12-6	4-6		
C7	G	12-7	4-7		
C8	H	12-8	4-8		
C9	I	12-9	4-9		
CA		12-0-9-8-2			CA through CF will not be assigned.
CB		12-0-9-8-3			
CC		12-0-9-8-4			
CD		12-0-9-8-5			
CE		12-0-9-8-6			
CF		12-0-9-8-7			
D0		11-0			D0 is unassigned.
D1	J	11-1	4-10		
D2	K	11-2	4-11		
D3	L	11-3	4-12		
D4	M	11-4	4-13		
D5	N	11-5	4-14		
D6	O	11-6	4-15		
D7	P	11-7	5-0		
D8	Q	11-8	5-1		
D9	R	11-9	5-2		
DA		12-11-9-8-2			DA through DF will not be assigned.
DB		12-11-9-8-3			
DC		12-11-9-8-4			
DD		12-11-9-8-5			
DE		12-11-9-8-6			
DF		12-11-9-8-7			
E0		0-8-2	11-0-9-1		E0, E1 are unassigned.
E1		11-0-9-1			
E2	S	0-2	5-3		
E3	T	0-3	5-4		
E4	U	0-4	5-5		
E5	V	0-5	5-6		
E6	W	0-6	5-7		
E7	X	0-7	5-8		
E8	Y	0-8	5-9		
E9	Z	0-9	5-10		
EA		11-0-9-8-2			EA through EF will not be assigned.
EB		11-0-9-8-3			
EC		11-0-9-8-4			
ED		11-0-9-8-5			
EE		11-0-9-8-6			
EF		11-0-9-8-7			
F0	0	0	3-0		
F1	1	1	3-1		
F2	2	2	3-2		
F3	3	3	3-3		
F4	4	4	3-4		
F5	5	5	3-5		
F6	6	6	3-6		
F7	7	7	3-7		
F8	8	8	3-8		
F9	9	9	3-9		
FA		12-11-0-9-8-2			FA through FE will not be assigned.
FB		12-11-0-9-8-3			
FC		12-11-0-9-8-4			
FD		12-11-0-9-8-5			
FE		12-11-0-9-8-6			
FF	DEL	12-11-0-9-8-7		delete	Special – neither graphic nor control symbol.

†Hexadecimal notation.

††Decimal notation (column-row).

APPENDIX B. PROGRAMMING EXAMPLES

SIGMA 5/7 PROGRAMMING EXAMPLE

The following partial program for a Sigma 5 or 7 computer illustrates the use of the I/O instructions and the card punch responses to these instructions. It is coded as a recursive routine that punches one card in the EBCDIC mode and then punches one card in the binary mode. The program does not use the interrupt system, but exits to another routine (not shown) that deals with specific error conditions. Note that the card punch is assumed to be in the "ready automatic" state when the SIO instruction is executed.

Label	Command	Argument	Comments
PNCARD	LI,0	DA(IOCD1)	Loads general register 0 with the doubleword address of the I/O control doubleword for the EBCDIC punch card operation.
	BAL,15	STARTIO	Causes a branch to a common punch routine, after which the next instruction will be executed.
	LI,0	DA(IOCD2)	Loads general register 0 with the doubleword address of the I/O control doubleword for the binary card punch operation.
	BAL,15	STARTIO	Causes a branch to a common punch routine, after which the next instruction will be executed.
	B	DONE	Causes a branch to another part of the program.
	⋮		
STARTIO	SIO,10	4	Starts the card punch (device 4 on IOP 0).
TESTIO	TIO,10	4	Obtains the I/O system and card punch status response.
	CW,11	BZTEST	Compares the I/O status response in register 11 with the "busy" test constant.
	BCS,4	TESTIO	Causes a branch back to the TIO instruction if the card punch is still "busy".
	CW,11	ERRCHK	Compares the I/O status response in register 11 with an error check constant.
	BCS,4	ERROR	Causes a branch to a routine that determines the reason for the error condition.
	B	*15	Causes a branch back to the main program.
Assembler Directives			
BZTEST	DATA	X'40000000'	Defines the "busy" test constant.
ERRCHK	DATA	X'23FE0000'	Defines the error check constant.
	BOUND	8	Establishes a doubleword boundary.
IOCD1	GEN 8,24 GEN 8,24	X'0D',BA(EBCDIC) X'08',80	Define the first I/O command doubleword for the card punch operation. The command doubleword specifies: EBCDIC punch, normal stacking, offset stacking on error, punch card image from area EBCDIC, halt on transmission error, and a byte count of 80.
IOCD2	GEN 8,24 GEN 8,24	X'09',BA(BINARY) X'08',120	Define the second I/O command doubleword for the card punch operation. The command doubleword specifies: binary punch, normal stacking, offset stacking on error, punch card image from area BINARY, halt on transmission error, and a byte count of 120.
EBCDIC	RES	20	Reserves 20 words (80 byte locations) for storage of the EBCDIC card image.
BINARY	RES	30	Reserves 30 words (120 byte locations) for storage of the binary card image.

SIGMA 2 PROGRAMMING EXAMPLE

The following partial program for a Sigma 2 computer illustrates the use of the I/O instructions and the card punch responses to these instructions. It is coded as a recursive routine that punches one card in the EBCDIC mode and then punches one card in the binary mode. The program does not use the interrupt system, but exits to another routine (not shown) that deals with specific error conditions. Note that the card punch is assigned to be in the "ready automatic" state when the SIO instruction is executed.

Label	Command	Argument	Comments
	⋮		
EVENREG	EQU	14	Establish the addresses of the even and odd channel registers.
ODDREG	EQU	15	
	⋮		
	LDA	=IOCD1	Loads register 7 with the address of the first I/O control doubleword.
	RCPY	7,5	Moves address to register 5, which will be used as base register in the common "STARTIO" routine.
	RCPYI	1,2	Saves return address.
	B	STARTIO	Branches to common "STARTIO" routine to punch a card in EBCDIC mode.
	LDA	=IOCD2	Program returns to this instruction after a successful EBCDIC punch operation. Loads register 7 with the address of the second I/O control doubleword.
	RCPY	7,5	Moves address to register 5, which will be used as base register in the common "STARTIO" routine.
	RCPYI	1,2	Saves return address.
	B	STARTIO	Branches to common "STARTIO" routine to punch a card in EBCDIC mode.
	B	DONE	Program returns to this instruction after a successful binary punch operation. Causes a branch to another part of the partial program.
	⋮		
STARTIO	LDA	0,0,1	Loads into register 7 the word address of the current I/O table pointed to by register 5.
	WD	*EVENREG	Sets this word address in the even channel register.
	RCPYI	5,5	Increments the base address by 1.
	LDA	0,0,1	Loads into register 7 the byte count for the next punch operation pointed to by register 5.
	WD	*ODDREG	Sets this byte count in the odd channel register.
	LDA	=4	Start the card punch (device 4).
	SIO		
TESTIO	LDA	=4	Obtain the I/O system and card punch status response.
	TIO		
	SCLS	1	Examines bit 1 of the response.
	BAN	TESTIO	If it is set, the device is still "busy".
	AND	ERRCHK	Saves, in register 7 only, any error bit defined by the mask called "ERRCHK".
	BAZ	RETURN	No error bits are reported in the status response.
	B	ERROR	One or more error bits are reported in the status response. Causes a branch to a routine that determines the reason for the error.
RETURN	RCPY	2,1	Returns to the calling program.
	⋮		

Label	Command	Argument	Comments
	:		
IOCD1	DATA DATA	IOTABLE1 81	First I/O control doubleword to be set in even and odd channel registers.
IOCD2	DATA DATA	IOTABLE2 121	Second I/O control doubleword to be set in even and odd channel registers.
ERRCHK	DATA	X'1C00'	Error check constant.
IOTABLE1	DATA RES	X'000D' 40	EBCDIC punch order. Forty words are reserved for the EBCDIC card image.
IOTABLE2	DATA RES	X'0009' 60	Binary punch order. Sixty words are reserved for the binary card image.